REMARKS

Applicants appreciate the Examiner's thorough review of the present application, and respectfully request reconsideration in light of the preceding amendments and the following remarks.

Claims 1-20 are pending in the application. Some of the original claims have been amended only to improve claim language without otherwise touching the merits. Claims 14-20 have been added to provide Applicants with the scope of protection to which they are believed entitled. The new claims find solid support in the original specification and drawings. No new matter has been introduced through the foregoing amendments.

The *35 U.S.C. 102(b)* rejection of claims 1-13 is traversed because the applied reference clearly fails to teach or disclose each and every element of the rejected claims.

With regard to claim 1, the claimed invention is distinctly different from the cited reference of *Lu et al.*, because the Examiner has mischaracterized **the interconnection layer** disclosed by the cited reference of *Lu et al.* as **the claimed connector.**

Lu et al. disclosed a multichip electronic packaging structure which comprises: a) a planar substrate having an upper surface; b) an array of flexible, electrically conductive interconnect members; c) a shell; d) a planar **interconnection layer** having an upper surface and a lower surface, said lower surface of said interconnection layer being electrically communicative with said array of interconnect members and affixed to said upper surface of said substrate; and e) **at least one device electrically and mechanically connected to said upper surface of said interconnection layer.** In col. 7, lines 25-30 of the cited reference, *Lu et al.* disclosed that **the device is bare dice or packaged device.** As shown in FIG. 5 of the cited reference, **the interconnection layer 550 is disposed between the substrate and the devices 512 (bare dice or packaged device) only for connecting the devices 512 (bare dice for packaged device) to the array of flexible, electrically**

conductive interconnect members 490.

However, present claim 1 recites that a package for electrically connecting to an external printed wiring board and an external electronic device comprises: a substrate electrically connected to the external printed wiring board; **a semiconductor chip** disposed on and electrically connected to the substrate; and **a connector disposed on the substrate for electrically connecting the semiconductor chip to the external electronic device.** The claim language finds solid support in the disclosure of the present invention. As shown in FIG.1 of the present application, **the connector 22 electrically connects the semiconductor chip 18 to the external electronic device (e.g. another external printed wiring board).** Thus, the interconnection layer disclosed by the cited reference is different from the claimed connector.

An advantage of the present invention has been disclosed in the specification: a semiconductor package with a connector having **a novel feature for being electrically connected to a plurality of external printed wiring boards or electronic devices in various directions**.

Accordingly, claim 1 is note anticipated by the cited reference of *Lu et al.* and is clearly patentable over the cited reference of *Lu et al.*

With regard to claim 4, the claimed invention is distinctly different from the cited reference of *Lu et al.*

In col. 7, lines 39-42 of the cited reference, *Lu et al.* disclosed that the interconnect layer 150 may be attached to the planar CTE controlled electronic substrate using an adhesive or polymer. It is apparent that the interconnect layer 150 is attached to the substrate by **using an adhesive or polymer, not by using a surface mount technology process.**

Accordingly, claim 4 is clearly patentable over the cited reference of *Lu et al.*

With regard to claims 2, 3, and 5-7, these claims depend from claim 1, and are considered patentable at least for the reason advanced with respect to claim 1.

With regard to claim 8, the claimed invention is distinctly different from the cited reference of *Lu et al.* The Examiner has mischaracterized **the interconnection layer 150 and the thermally conductive shim 120** disclosed by the cited reference of *Lu et al.* as **the claimed first substrate and connector, respectively**.

As shown in FIG. 1 of the cited reference, *Lu et al.* disclosed that **the interconnection layer 150 is disposed between the substrate and the devices 110 (bare dice or packaged device) only for connecting the devices 110 (bare dice or packaged device) to the array of flexible, electrically conductive interconnect members 590**. Furthermore, *Lu et al.* disclosed that **the thermally conductive shim 120 is disposed between the metallized package cover 140 and the devices 110 (bare dice or packaged device)**.

However, present claim 8 recites a package for electrically connecting to an external printed wiring board and an external electronic device comprising: a first substrate; a first semiconductor chip electrically connected to the first substrate; a second substrate; a second semiconductor chip electrically connected to the second substrate; a medium substrate electrically connected to the first substrate and the second substrate; and a connector electrically connected to the first substrate and the second substrate, wherein **the first substrate is electrically connected to the external printed wiring board and the connector is electrically connected to the external electronic device**. The claim language finds solid support in the disclosure of the present invention. As shown in FIG. 4 of the present application, **the first substrate 58 is electrically connected to the external printed wiring board, the first semiconductor chip 54, the medium substrate 68 and the connector 70**. Furthermore, the description of preferred embodiments of the present invention discloses that **the connector 70 is electrically connected to the external electronic device (e.g. another external printed wiring board), the first substrate 58 and the second substrate 56**. Thus, the interconnection layer 150 and the thermally conductive shim 120 disclosed by the cited reference of

Lu et al. is different from the claimed first substrate and connector.

Accordingly, claim 8 is not anticipated by the cited reference of *Lu et al.* and is clearly patentable over the cited reference of *Lu et al.*

With regard to claim 11, the claimed invention is distinctly different from the cited reference of *Lu et al.* Note the discussion of claim 4.

With regard to claim 9, 10 and 12-13, these claims depend from claim 8, and are considered patentable at least for the reason advanced with respect to claim 8.

With regard to claim 14, the claimed invention is distinctly different from the cited reference of *Lu et al.* Note the discussion of claim 1.

New claims 15-20 depend from claim 1 or 8, and are considered patentable at least for the reasons advanced with respect to claims 1 and 8. Claims 5-20 are also patentable on their own merits since these claims recite other features of the invention neither disclosed, taught nor suggested by the applied art, as will be apparent to the Examiner upon reviewing these claims.

Each of the Examiner's rejections has been traversed. Accordingly, Applicants respectfully submit that all claims are now in condition for allowance. Early and favorable indication of allowance is courteously solicited.

The Examiner is invited to telephone the undersigned, Applicant's attorney of record, to facilitate advancement of the present application.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 07-1337 and please credit any excess fees to such deposit account.

Respectfully submitted,

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